Application Note 610
Replacing an Atmel TS80C51U2 with a DS80C320/323

www.maxim-ic.com

INTRODUCTION

Dallas Semiconductor developed an innovative family of 8051 microcontrollers running at 4 clocks-per-machine cycle instead of the original 12 clocks. While some of the instructions increased in machine cycles, the overall improvement in performance achieved by most applications will be 2.5X. The Atmel 8051 family runs at 6 clocks-per-machine cycle, compared to the original 12, without increasing the number of machine cycles per instruction. This results in an improvement of 2X over the original 8051 architecture. The DS80C320 also contains several feature enhancements over the original 8051 including dual data pointers, power-management mode, enhanced watchdog timer, a ring oscillator, and stretch cycles for external memory (MOVX) access.

The purpose of this application note is to provide information on converting application code from the Atmel TS80C51U2 to the faster DS80C320.

FEATURES

Table 1. DS80C320/323 vs. TS80C51U2

FEATURE	DESCRIPTION	DALLAS	ATMEL
Maximum Operating Frequency 4.5V to 5.5V		33MHz (82.5MHz equivalent)	30MHz (60MHz equivalent)
Maximum Operating Frequency 2.7V to 5.5V		18MHz (45MHz equivalent)	20MHz (40MHz equivalent)
MOVX Stretch	Stretch external data read/write to allow access to slower peripherals	Y	N
External Interrupt Sources		6	2
Four I/O Ports	Ports 0, 1, 2, 3	Y	Y
Three 16-Bit Timer/Counters	Timer 0, 1, 2	Y	Y
256 Bytes Internal RAM		Y	Y
Dual Data Pointer	DPTR0, DPTR1	Y	Y
Power Saving Modes	Idle mode, sleep	Y	Y
Power-Fail Reset	Brownout detector	Y	N
Power-Fail Warning	Early power-fail warning interrupt	Y	N
Programmable Watchdog Timer		Y	Y
Watchdog Interrupt		Y	N
Interrupt Priority Levels	Programmable interrupt levels	2	4
Two Full-Duplex Serial UARTs	7 or 8 data bits, 1 or 2 stop bits, parity, framing error recognition, address recognition	Y	Y

REV: 021803

PINOUT

Table 2. DS80C320/323 and TS80C51U2 Pinout Differences

PIN			NAME	DIFFERENCE IN DS80C320	DESCRIPTION/COMMENT		
DIP	PLCC	TQFP, VQFP					
20	22, 23	16, 17	V_{SS}	Two ground connections provided	On TS80C51U2, PLCC pin 23 and VQFP44 pin 17 are N.C. These pins can be left floating on the DS80C320/323 without problems.		
9	10	4	RST		Reset. DS80C320/323 does not require an external capacitor, however, if one is placed it does not affect behavior.		
					Alternate	**Function**	**Comment**
3	4	42	P1.2	No difference (Note 1)	RXD1	Serial port 1 Input	
4	5	43	P1.3	No difference (Note 1)	TXD1	Serial port 1 Output	
5	6	44	P1.4	Can be used as external interrupt	INT2	External Interrupt	TS80C51U2 only has two external interrupts.
6	7	1	P1.5	Can be used as external interrupt (Note 1)	$\overline{INT3}$	External Interrupt	TS80C51U2 only has two external interrupts.
7	8	2	P1.6	Can be used as external interrupt (Note 1)	INT4	External Interrupt	TS80C51U2 only has two external interrupts. Can be serial 1 output on TS80C51U2.
8	9	3	P1.7	Can be used as external interrupt (Note 1)	$\overline{INT5}$	External Interrupt	TS80C51U2 only has two external interrupts. Can be serial 1 output on TS80C51U2
—	12	6	N.C.	No Connect	Optional serial port1 input on TS80C51U2 (Note 1)		
—	34	28	N.C.	No Connect	Optional serial port1 output on TS80C51U2 (Note 1)		
—	1	39	N.C.	No Connect	V_{SS} on TS80C51U2, grounding pin on DS80C320/323 causes no problems		

Note 1: TS80C51U2 serial port 1 input/output can be located on different positions, depending on AUXR bit M1UA1 and M0UA_1 bit.

SFR MEMORY MAP

Table 3. SFR Differences

REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	ADDR	COMMENT
DPL1									84H	TS80C51U2 DPL1/DPL use SFR address 82h (DPL on DS80C320/323).
DPH1									85H	TS80C51U2 DPH1/ DPH use SFR address 83h (DPH on DS80C320/323).
DPS	0	0	0	0	0	0	0	SEL	86H	TS80C51U2 uses DPS bit in AUXR1 SFR.
CKCON DS80C320/ 323	WD1	WD0	T2M	T1M	T0M	MD2	MD1	MD0	8Eh	WD1,0 watchdog timeout. See Watchdog Section T2M, T1M, T0M (timer speed); See Timer Section MD2, MD1, MD0 (Stretch MOVX)
AUXR TS80C51U2	M1UA_1	M0UA_1	—	—	—	—	—	A0		TS80C51U2 does not support stretch. M1UA_1/M0UA_1 on TS80C51U2 selects UART1 pin out.
CKCON TS80C51U2 only								X2	8Fh	12/6 clock select on TS80C51U2, register not used on DS80C320/323.
EXIF	IE5	IE4	IE3	IE2	—	RGMD	RGSL	BGS	91h	IE5, 4, 3, 2 Additional external interrupts supported by DS80C320/323.
BRL TS80C51U2 Only	BRL7	BRL6	BRL5	BRL4	BRL3	BRL2	BRL1	BRL0	9Ah	Baud rate generator on TS80C51U2. Register not used on DS80C320/323.
BDRCON TS80C51U2	—	—	—	BRR	TBCK_0	RBCK_0	SPD	SRC	9Bh	See serial port baud section below.
BDRCON_1 TS80C51U2	SMOD1_1	SMOD0_1	RCLK_1	TCLK_1	TBCK_1	RBCK_1	—	—	9Ch	See serial port baud section below.
AUXR1 TS80C51U2	—	—	—	—	—	—	—	DPS	A2h	DPS select is handled in register DPS.0 on DS80C320/323.
WDTRST TS80C51U2									A6h	Watchdog reset handled in WDCON register on DS80C320/323.
WDTPRG TS80C51U2	T4	T3	T2	T1	T0	S2	S1	S0	A7h	Watchdog timeout handled in

REGISTER	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0	ADDR	COMMENT
										CKCON register on DS80C320/323.
IPH TS80C51U2	—	PSH_1	PT2H	PSH_0	PT1H	PX1H	PT0H	PX0H	B7h	Interrupt priorities handled in IP and EIP registers on DS80C320/323.
STATUS	PIP	HIP	LIP	1	1	1	1	1	C5h	Interrupt status for clock control. Not present in Atmel TS80C51U2.
TA									C7h	Timed Access Control
EIE	—	—	—	EWD1	EX5	EX4	EX3	EX2	E8h	Enable watchdog interrupt and enable extended interrupts. Additional features not supported on TS80C51U2.
EIP	—	—	—	PWDI	PX5	PX4	PX3	PX2	F8h	Watchdog interrupt and extended interrupts. Additional features not supported on TS80C51US.

DUAL DATA POINTERS

Unlike the Atmel TS80C51U2 that uses shadow registers, the DS80C320/323 maps the two data pointers to different registers. DPL0 is at SFR address 82h, DPH0 is at 83h, DPL1 is at 84h, and DPH1 is at 85h. DPL is mapped at SFR 82h and DPH is at SFR 83h on the Atmel TS80C51U2. To toggle between the active DPTR on the DS80C320/323, use DPS.0 instead of AUXR1 on the TS80C51U2. Having separate registers for the dual data pointers allows access to either set of registers without having to change the active DPTR.

WATCHDOG TIMER

The Dallas DS80C320/323 implements an advanced watchdog reset with support for a watchdog interrupt prior to reset of the device on expiration of the timer. The watchdog interrupt vector is located at 63h and is vectored to 512 cycles prior to the watchdog timeout. An application can either reset the watchdog and hold off the reset or it can perform clean-up functions and let the reset happen at the end of the 512 cycles.

The WD1 and WD0 bits in the CKCON register control the watchdog timeout values. Table 4 shows the possible settings. Prior to changing the values of the WD1 and WD0 bits, the reset watchdog timer bit (WDCON.0) should be set to avoid corruption of the watchdog count. Setting the EWDI (EIE.4) bit enables the watchdog timer interrupt and the EWT (WDCON.1) enables the watchdog timer. To reset the watchdog timer, application code sets the RWT (WDCON.0) bit. To avoid a watchdog timeout, this bit must be set by application code prior to the timeout. Timed access, DS80C320/323 data sheet page 18, protects both the watchdog enable and the watchdog reset bits, preventing runaway code from accidentally resetting or disabling the watchdog timer.

Table 4. Watchdog Settings

WD1	WD0	INTERRUPT TIMEOUT	TIME (ms) (AT 33MHz)	RESET TIMEOUT	TIME (ms) (AT 33MHz)
0	0	2^{17} clocks	3.97	2^{17} + 512 clocks	4
0	1	2^{20} clocks	31.76	2^{20} + 512 clocks	31.79
1	0	2^{23} clocks	254.2	2^{23} + 512 clocks	254.22
1	1	2^{26} clocks	2034	2^{26} + 512 clocks	2037

The SFR register WDTRG bits S0, S1, and S2 program the TS80C51U2 watchdog timeout period. The timeout is programmable from 3.26ms to 418ms at 30MHz. The Atmel microcontrollers require that a 1Eh and then an E1h be written to the WDTRST SFR to enable or reset the timer.

TIMERS

The DS80C320/323 allows timers 0, 1, and 2 to be run in original 8051 Xtal/12 or from Xtal/4 mode. To run in the 4-clock timer mode, T2M, T1M, or T0M bits must be set for each timer. Unlike the TS80C51U2, the timers can be set independently to run in either 12- or 4-clock mode. This allows the DS80C320/323 more flexibility in timer rates. On the TS80C51U2, all timers either run in 6-clock or 12-clock mode depending on the X2 bit in CKCON.

The reload values for each timer must be recalculated to account for the difference in Xtal/6 or Xtal/4 modes. Refer to the DS80C320/323 data sheet for detailed functions for calculating the reload values.

PCON UART CONTROL

Both the DS80C320/323 and the TS80C51 allow baud-rate doubling and framing-error detection. The baud-rate doubling flags for the DS80C320/323 are SMOD_0 in PCON and SMOD_1 in WDCON. Setting these bits enables baud-rate doubling. To enable framing-error detection set SMOD0 (PCON.6).

UART

The TS80C51U2 includes a dedicated baud-rate generator that is not available in the DS80C320/323. It is necessary to convert serial code that uses the baud-rate generator to use an available timer. Refer to the *High-Speed Microcontroller User's Guide* for specifics on baud-rate generation with the timers (Section 12.3).

INTERRUPTS

The DS80C320/323 provide 2 levels of interrupt priority with natural priority selection. Table X shows the priority levels of the DS80C320/323 compared to the TS80C51U2.

Note: The TS80C51 serial port 1 interrupt vector is located at address 33h. On the DS80C320/323 the serial port 1 interrupt vector is located at 3Bh and the power-fail interrupt is at 33h.

Table 5. Interrupt Priorities

NAME	DALLAS LEVEL	ATMEL LEVEL	VECTOR	COMMENT
Power-Fail Indicator	1	Not Available	33h	Warning ATMEL serial port 1 interrupt vector
External Interrupt 0	2	1	03h	
Timer 0 Overflow	3	2	0Bh	
External Interrupt 1	4	3	13h	
Timer 1 Overflow	5	4	1Bh	
Serial Port 0	6	5	23h	
Timer 2 Overflow	7	6	2Bh	
Serial Port 1	8	7	3Bh	Warning ATMEL serial port 1 vector at 33h
External Interrupt 2	9	Not Available	43h	
External Interrupt 3	10	Not Available	4Bh	
External Interrupt 4	11	Not Available	53h	
External Interrupt 5	12	Not Available	5Bh	
Watchdog Interrupt	13	Not Available	63h	

RESET AND POWER-FAIL

The DS80C320/323 includes an internal bandgap reset circuit, which monitors voltage on V_{CC} to ensure that the proper operation levels are maintained. If the operating voltage falls past the power-fail warning level, a power-fail interrupt is triggered, which allows application code to cleanly shut down the system. The Atmel TS80C51U2 does not include a bandgap reset, and typically requires the usage of an external IC for this purpose, increasing overall cost, part count, and operating current.

Maxim Integrated Products/Dallas Semiconductor Contact Information

Company Addresses:

Maxim Integrated Products, Inc.
120 San Gabriel Drive
Sunnyvale, CA 94086
Tel: (408) 737-7600
Fax: (408) 737-7194

Dallas Semiconductor
4401 S. Beltwood Parkway
Dallas, TX 75244
Tel: (972) 371-4448
Fax: (972) 371-4799

Product Literature/Samples Requests:
(800) 998 - 8800
(408) 737 - 7600

Sales and Customer Service:

World Wide Website:
www.maxim-ic.com

Product Information:
www.maxim-ic.com/MaximProducts/products.htm

Ordering Information:
www.maxim-ic.com/BuyMaxim/Sales.htm

FTP Site:
ftp://ftp.dalsemi.com